#6/B 2814

PATENTS

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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

M. Brunson 2/12/03

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| In re Application of: | |
| **Makoto Yamamoto** | |
| | Art Unit: **2814** |
| Serial No. **10/014,949** | |
| | Examiner: **Shrinivas H. Rao** |
| Filed: **October 26, 2001** | |
| For: **Lateral Transistor Having Graded Base Region, Semiconductor Integrated Circuit And Fabrication Method Thereof** | |



**SECOND RESPONSE**

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

Responsive to the Final Office Action dated September 24, 2002 in the patent application identified above, please enter the following amendments and reconsider this application in view of the appended remarks.

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, DC 20231, on December 24, 2002.

Roger T. Frost

Roger T. Frost- Reg. No. 22,176